

Figure 1A

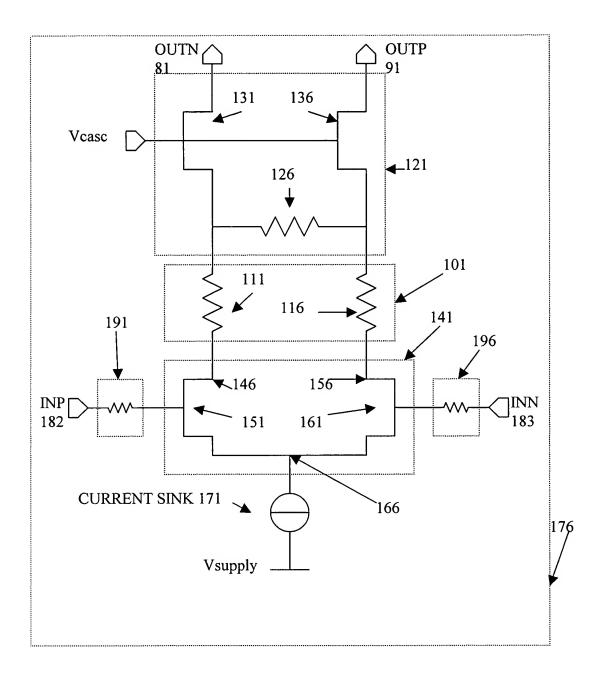


Figure 1B

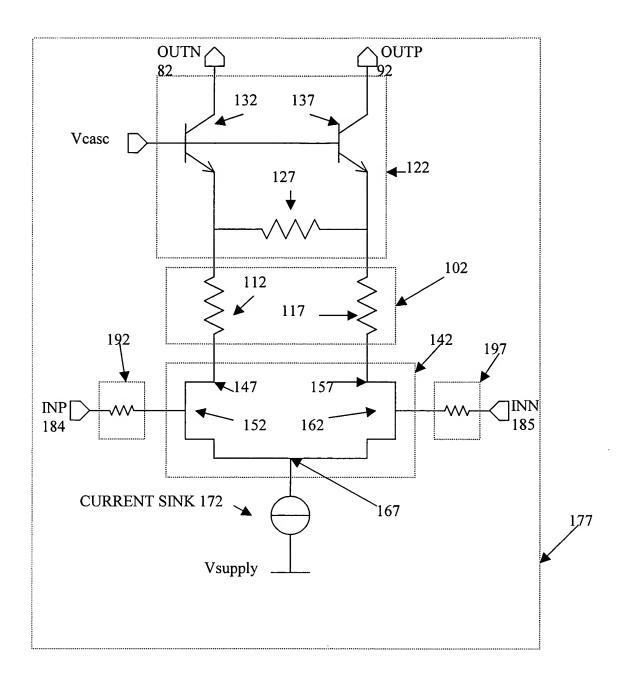


Figure 1C

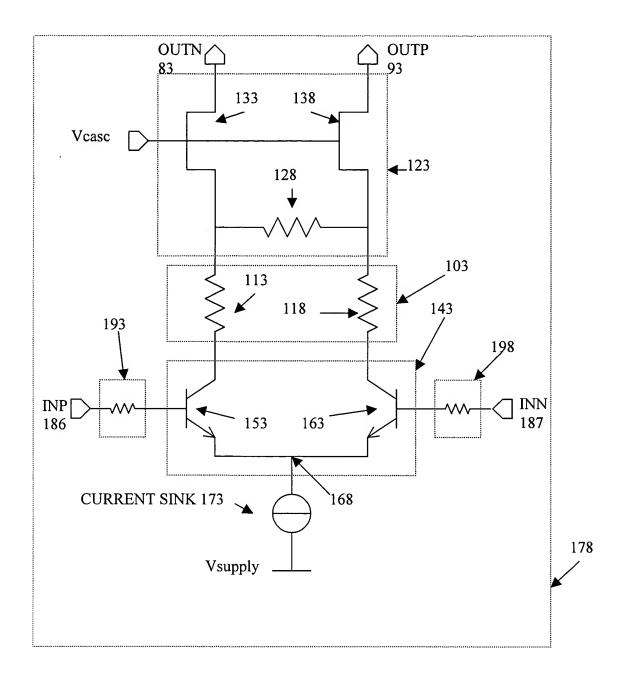


Figure 1D

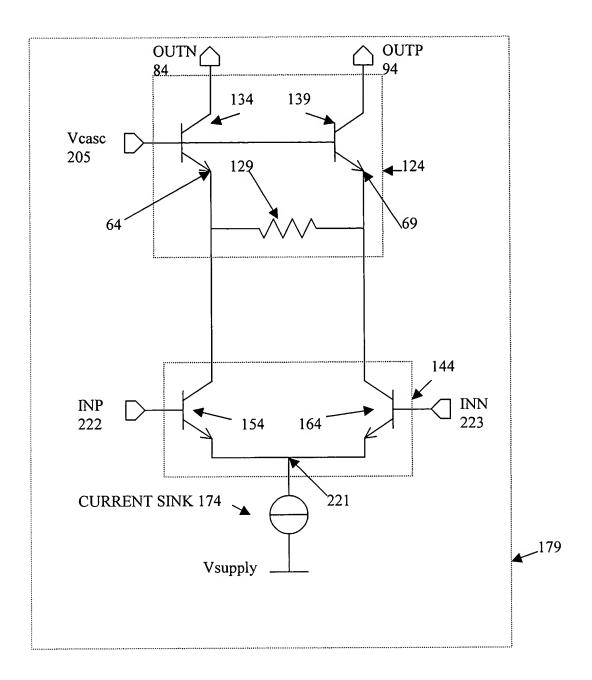


Figure 2

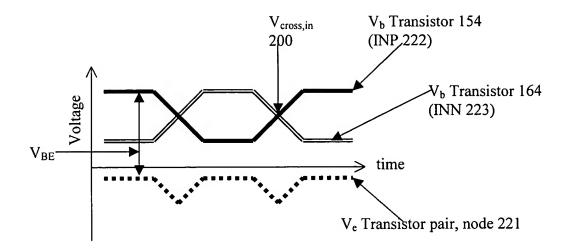


FIG 3a

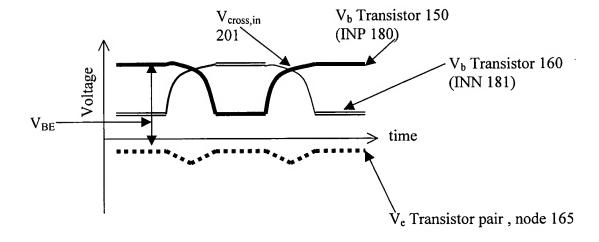


FIG 3b

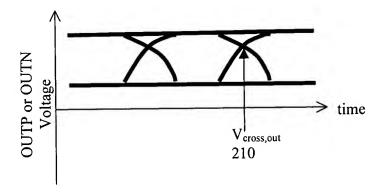


FIG 4a

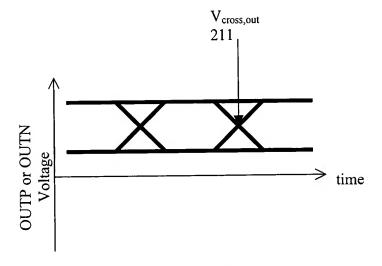


FIG 4b

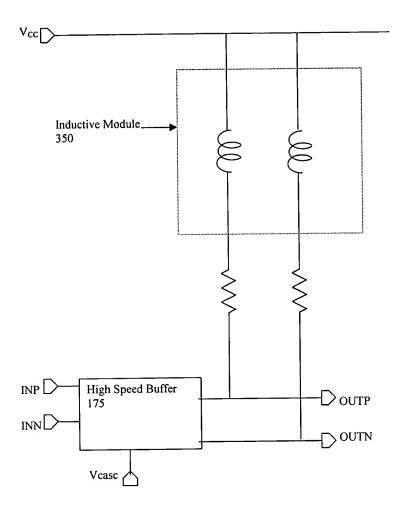


Figure 5

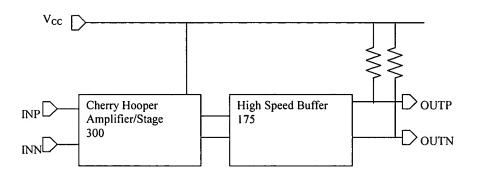


Figure 6

A cascode transistor module is established (S1).

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The resistive loads seen by the output nodes of the differential pair module are engineered to optimize the eye diagram shape or the $V_{cross,out}$ of the output signals of the cascode transistor module (S2).

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Optionally, an optional cascode resistive module is used to alter the resistive loads seen by the output nodes of the differential pair module to further optimize the eye diagram shape or the $V_{cross,out}$ (S3).

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Optionally, the resistance associated with the stage driving the differential pair is carefully selected (S4).

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Optionally, the signal input to the differential pair module is preconditioned (S5).

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Optionally, the output signals of the cascode transistor module are coupled to an inductive module (S6).